

MITX-BYT80 Motherboard

User Manual

Chapter 1: Introduction

1.1 Parameters

Platform: Onboard Intel Bay Trail-D Celeron J1800 processor, 2.41GHZ, dual core, TDP 10W.

Onboard Intel Bay Trail-D Celeron J1900 processor, 2.0GHZ, quad core, TDP 10W.

System memory: single channel DDR3L-1333MHZ up to memory of 8GB.

GPU: Integrated Intel HD Graphics.

Display: 1 x VGA, a set of eDP pins(2 LANES), a set of dual channel 24 bit LVDS pins(it can be set as eDP).

Storage: 2 x SATA2.0, 1 x mSATA(mSATA and SATA2 are alternatives).

USB: 1 x USB3.0, 7 x USB2.0(4 is the pin).

LAN: Onboard 1 x gigabit LAN.

Audio: High resolution audio chip ALC662; supports Speaker-out, MIC-in, front audio and dual channel audio power amplifier(SPDIF-out is optional).

I/O: supports 6 x COM ; 1 x LPT(DB-25), PS/2, KB/MS.

Other I/O: 1 x MINI-PCIE (supports WIFI, supports 3G/4G network with optional SIM card slot), (mSATA slot can be configured as mini PCIE slot, supports a maximum of two mini-PCIE devices)

Size: 170mm x 170mm.

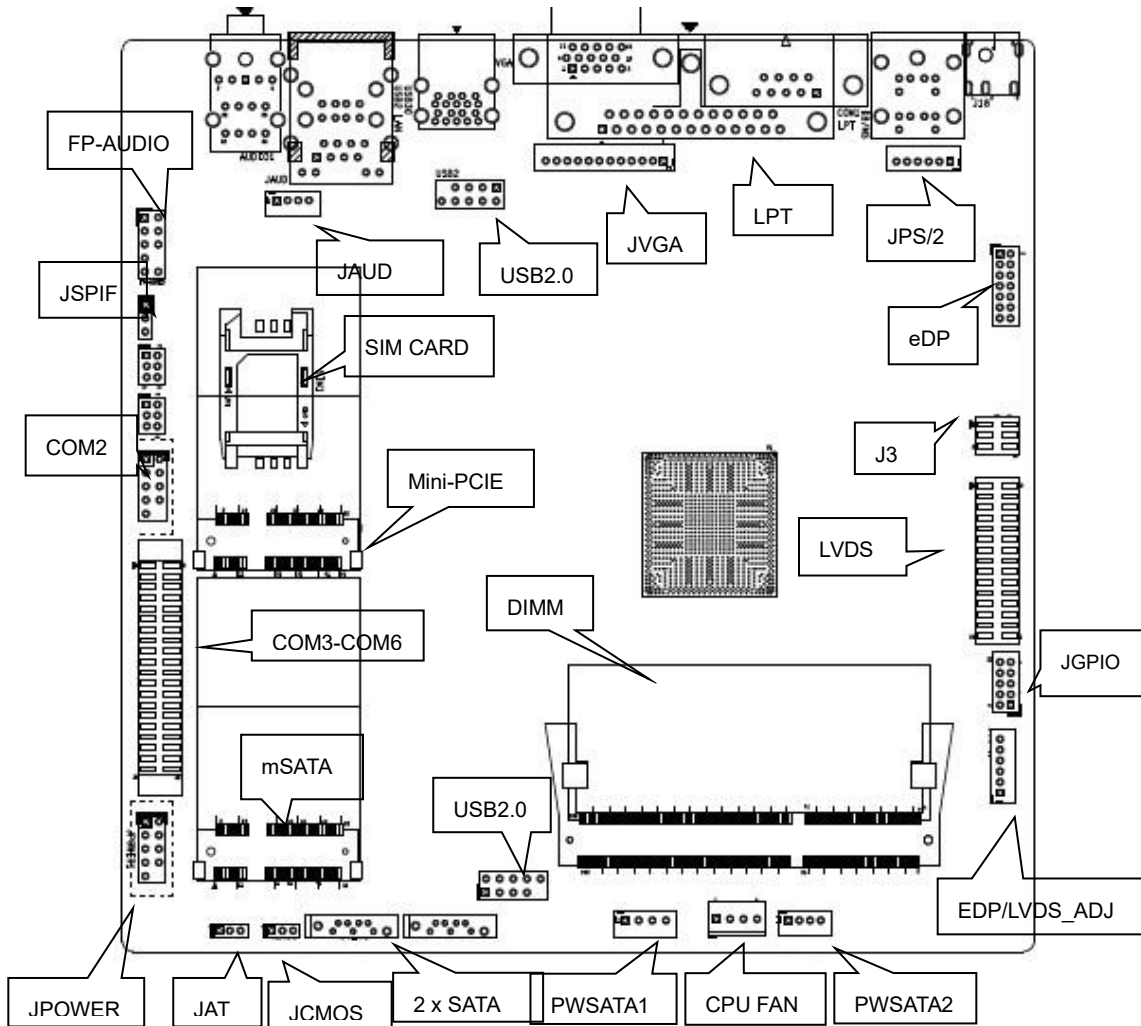
Power:DC-IN adapter (12V)

Operating Temperature: -40°C-60°C.

 Do not power this board with adapters or power of other voltage.

Chapter 2: Hardware

1.2 Interfaces



⚠ Please carefully read this manual before you connect an external connector, so as to avoid damage to the board.

2.1 Jumper Setting

Tips (ways to identify the first pin): Indicated by “1” or bold line or triangle symbol ; the square pad on the back of the bolding pad.

2.2 System Memory Slot

1 x DDR3L-1333MHZ SO-DIMM slot with up to 8GB memory, voltage is 1.35V.

2.3 Built-in Display Interface

1 x VGA(pins reserved), a set of 1.3 eDP pins(2 LANES), a set of dual channel 24bit LVDS pins(1.3 eDP is an alternative), supports independent dual display.

2.4 VGA(Silk Printed:JVGA)

VGA pin plug is reserved as an alternative plan.

VGA pin plug and rear standard VGA plug can not be connected to the screen simultaneously.

JVGA:

Pin	Signal
1	CRT_DDC_ DATA
2	CRT_DDC_ CLK
3	GND
4	VGA_B_R
5	GND
6	VGA_G_R
7	GND
8	VGA_R_R
9	GND
10	CRT_HSYNC1
11	CRT_VSYNC1
12	VGA_DVI_5V

2.5 eDP pin (Silk Printed:JEDP)

JEDP:

Signal	Pin		Signal
VCC	1	2	VCC
GND	3	4	EDP_DETECT
EDP_TX0_DP	5	6	EDP_BKLON
EDP_EX0_DN	7	8	EDP_BKLADJ
GND	9	10	GND
EDP_TX1_DP	11	12	EDP_AUXP
EDP_EX1_DN	13	14	EDP_AUXN

GND	15	16	GND
+12V	17	18	+12V

2.6 LVDS(Silk Printed:EDP/LVDS, EDP/LVDS_ADJ1, J3)

There is a dual channel 24bit LVDS. The VCC power of LVDS screen cable is controlled by J3, and EDP/LVDS_ADJ1 is controlled by the backlight power.

LVDS (Silk Printed:EDP/LVDS) :

Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	GND
GND	5	6	GND
A_DATA0_DN	7	8	A_DATA0_DP
A_DATA1_DN	9	10	A_DATA1_DP
A_DATA2_DN	11	12	A_DATA2_DP
GND	13	14	GND
A_CLK_DN	15	16	A_CLK_DP
A_DATA3_DN	17	18	A_DATA3_DP
B_DATA0_DN	19	20	B_DATA0_DP
B_DATA1_DN	21	22	B_DATA1_DP
B_DATA2_DN	23	24	B_DATA2_DP
GND	25	26	GND
B_CLK_DN	27	28	B_CLK_DP
B_DATA3_DN	29	30	B_DATA3_DP

LVDS backlight pin(Silk Printed:EDP/LVDS_ADJ1):

Pin	Signal
1	12V
2	12V
3	LCD_BKL_ON
4	LCD_BKL_ADJ
5	GND

6	GND
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LVDS voltage pin(Silk Printed:J3):

Pin	Setting	Function
1-2	Close	VCC(+3.3V)
3-4	Close	VCC(+5V)
5-6	Close	VCC(+12V)

Attention: LVDS screen's power can be adjusted among 12V/5V/3.3V via jumper setting according to your LVDS screen's voltage(Connecting 2 or more interfaces via jumper cap at the same time is strictly forbidden).

2.7 Optional eDP(Silk Printed:EDP/LVDS, EDP/LVDS_ADJ1, J3)

Supports 1.3 eDP of 2 LANES.

When set as eDP, LVDS's function will be canceled.

The LVDS screen power is controlled by J3, and EDP/LVDS_ADJ1 is controlled by the backlight power.

eDP pin (Silk Printed:EDP/LVDS) :

Signal	Pin		Signal
VCC	1	2	VCC
VCC	3	4	EDP_HPD
GND	5	6	GND
EDP_AUXN	7	8	EDP_AUXP
N/A	9	10	N/A
EDP_DATA0_P	11	12	EDP_DATA0_N
GND	13	14	GND
N/A	15	16	N/A
EDP_DATA1_P	17	18	EDP_DATA1_N
N/A	19	20	N/A
N/A	21	22	N/A
N/A	23	24	N/A

GND	25	26	GND
N/A	27	28	N/A
N/A	29	30	N/A

eDP backlight pin(Silk Printed:EDP/LVDS_ADJ1):

Pin	Signal
1	12V
2	12V
3	LCD_BKL_ON
4	LCD_BKL_ADJ
5	GND
6	GND

eDP voltage pin(Silk Printed:J30)

Pin	Setting	Function
1-2	Close	VCC(+3.3V)
3-4	Close	VCC(+5V)
5-6	Close	VCC(+12V)

⚠ Attention: LVDS screen's power can be adjusted among 12V/5V/3.3V via jumper setting(Connecting 2 or more interfaces via jumper cap at the same time is strictly forbidden).

2.8 LAN

RTL8111F Chip, 1 x RJ45. supports Wake On Lan and PXE.

RJ45 LAN LED:

LILED (green)	Description	ACTLED (yellow)	Description
ON	Connected	Flashing	Data transmitting

2.9 Audio

ALC662 audio chip; the green one is for Speaker-out, and the pink one is for Mic in; JAUD for Amplifier out; JSPIF for SPDIF OUT(optional).

FP_AUDIO(Silk Printed: FP_AUDIO):

Signal	Pin		Signal
MIC2-L	1	2	AGND
MIC2-R	3	4	AVCC
FRO-R	5	6	MIC2-JD
F-IO-SEN(AGNG)	7	8	(NC)
FRO-L	9	10	LIN2-JD

JAUD

Pin	Signal
1	L+
2	L-
3	R-
4	R+

SPDIF-out((Silk Printed:JSPIF)

Pin	Signal
1	+5V
2	SPDIF Out
3	GND

2.10 Build-in USB interface(USB1、 USB2)

Two sets of USB2.0 pins with expansion to 4 USB2.0 interfaces.

USB1、 USB2:

Signal	Pin		Signal
5V	1	2	5V
USB DATA-	3	4	USB DATA-
USB DATA+	5	6	USB DATA+
GND	7	8	GND

(NUL)	9	10	(NC)
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2.11 Serial Port (COM1、JCOM2、JCOM36、JCOM2_P、JCOM4_P)

6 x RS232 COM; COM1 is a standard interface(DB-9) and other Com are pins on board.

JCOM2_P and JCOM4_P provide voltage (5V/12V optional) for COM2 and JCOM4.

JCOM2:

Signal	Pin		Signal
DCD#	1	2	RXD
TXD	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS#
RI#	9	10	(NC)

JCOM36:

Signal	Pin		Signal
DCD#	1	2	RXD
TXD	3	4	DTR#
GND	5	6	DSR#
RTS#	7	8	CTS#
RI#	9	10	(NC)
DCD#	11	12	RXD
TXD	13	14	DTR#
GND	15	16	DSR#
RTS#	17	18	CTS#
RI#	19	20	(NC)
DCD#	21	22	RXD
TXD	23	24	DTR#
GND	25	26	DSR#
RTS#	27	28	CTS#
RI#	29	30	(NC)
DCD#	31	32	RXD

TXD	33	34	DTR#
GND	35	36	DSR#
RTS#	37	38	CTS#
RI#	39	40	(NC)

JCOM2_P、JCOM4_P:

Pin	Setting	Function
1-2	Close	5V
3-4	Close	RI
5-6	Close	12V

⚠ Do not short-circuit the 3 sets at the same time.

2.12 SATA and mSATA (Silk Printed:MSATA、SATA1、SATA2、PWSATA1、PWSATA2)

2 x SATA2.0 and 1 x mSATA(SATA2 and mSATA are alternatives)

2 x 4pin hard disk power interfaces, silk printed as PWSATA1、PWSATA2:

Pin	Signal
1	+5V
2	GND
3	GND
4	+12V

2.13 Mini-PCIE (Silk Printed:MINI-PCIE, SIM1)

Connects wifi, it can connect 3G/4G network with SIM card.

mSATA can be set as Mini PCIE, so the board can support a maximum of 2 MINI-PCIE devices (In this case, mSATA's function is canceled.)

2.14 GPIO(Silk Printed: JGPIO)

One 2×5Pin JGPIO(2.0mm distance),8 programmable I/O interfaces

Signal	Pin	Signal

GPI_S5_0 5_0	1	2	1.8V
GPI_S5_1	3	4	GPO_S5_6
GPI_S5_2	5	6	GPO_S5_7
GPI_S5_3	7	8	GPO_S5_8
GND	9	10	GPO_S5_9

2.15 Power supply (Silk Printed:J18)

Only supports DC-IN adapter (12V)



2.16 Front Panel Interface (Silk Printed:JPOWER1)

Front-face panel interface is to connect function buttons and indicator lights on the case.

JPOWER1:

Signal	Pin		Signal
HDD_LED+	1	2	PWR_LED+
HDD_LED-	3	4	PWR_LED-
RSTBTN+	5	6	PWR_ON+
RSTBTN-	7	8	PWR_ON-
NUL	9	10	(NC)

2.17 PS/2 KB/MS (Silk Printed:PS2_H)


6pin PS/2 socket provided

Pin	Signal
1	+5V
2	KB_DATA
3	KB_CLK
4	MS_DATA
5	MS_CLK
6	GND

2.18 Auto Power On (Silk Printed:JAT)

JAT:

Pin	Setting	Function
1-2	Close	AUTO START
2-3	Close	NC

 **Note:** This function shares some similarity with “Restore AC Power Loss” in BIOS. If the latter is set to be “Power on”, this function will automatically be on.

2.19 CMOS ((Silk Printed:JCMOS)

CMOS is powered by the button battery on the board. Clearing CMOS will permanently clear previous system setting and restore it to factory setting.

Steps: 1. Power the computer off;

2. Short-circuit the jumper cap to the 1st and 2nd pin of JCMOS for 10 secs, and disconnect;

3. Turn on the computer and press to enter BIOS setting, overload the best default value;

4. Save and exit.

JCMOS:

Pin	Setting	Function
1-2	Close	CLR CMOS
2-3	Close	NC

 **Do not clear CMOS when the computer is connected to power.**